REMARKS

Claims 1-9 are currently pending in the application. Claim 6 has been amended. New claim 9 has been added. Claims 3-5 were objected to but were indicated as being allowable if rewritten in independent form, including all of the limitations of the base claim and any intervening claims.

On page 2 of the Office Action, claims 6 and 7 were objected to under 37 C.F.R. § 1.75(c) as being in improper form. Applicants have amended claim 6. Therefore, withdrawal of the rejection is respectfully requested.

On page 2 of the Office Action, claims 1 and 2 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,831,883 (Suter) in view of U.S. Patent No. 5,694,347 (Ireland).

Suter is directed to a practical, low-energy consumption method of performing an N-point fast Fourier transform employing multirate, parallel and asynchronous circuit design techniques. According to Suter, the multirate feature allows an input data sequence to be broken down into its polyphase components. As illustrated in Fig. 1 of Suter, the apparatus thereof may adopt two stages, that is, the preceding stage and succeeding stage. In Suter, however, where a transform point number $M = N_1 \times N_2$, the number of the N_1 point FFT means of the preceding stage is N_2, and the number of the N_2 point FFT means of the succeeding stage is N_1. Suter also needs to use an asynchronous circuit that is free of a global clock.

Ireland is directed to a signal processing system in which a memory is included for storing an N-point sequence of input data points and corresponding coefficient values. A processor is also included for computing the Fast Fourier Transform of the N-point sequence of input data points. The processor consists of a series of (L) individual radix 2 processing stages, where $L = \log_2 N$, and N is a number of input data points. *See* Ireland, column 2, lines 60-63.

In the present invention, each of the M-point radix 2 pipeline FFT circuits has two parallel inputs/outputs, wherein $M = 2^m$, m>=2, and represents a maximum number of points for transform. Fourier transform apparatus of the present invention has the pipeline width which is independent of transform point number of individual pipeline FFT circuits in each stage, thereby providing a large number of FFT transform points and high throughput.

Applicants respectfully submit that independent claim 1 is patentable over the references, as neither Suter nor Ireland, alone or in combination, teaches or suggests, "M-point

radix 2 pipeline FFT circuits with two parallel inputs/outputs," wherein "M" represents a maximum number of points for transform and is equal to 2^m, m>=2, as recited in independent claim 1.

On page 2 of the Office Action, the Examiner noted that Suter does not specifically disclose a transform means having radix 2 pipeline FFT circuits and the twiddle factor multiplication means including 2a complex multiplication circuits as claimed. The Examiner alleged, however, that Ireland discloses an M-point radix 2 pipeline FFT circuit.

Applicants respectfully submit that in contrast to the present invention and contrary to the Examiner's allegation, Ireland does not teach *M-point* radix 2 pipeline FFT circuits. Rather, Ireland teaches *N-point* fast Fourier transform. *See* Ireland, column 4, lines 42-44. In Ireland "N" is simply the number of input data points and does not represent a maximum number of points for transform, as in the present invention. Moreover, Ireland specifically states that the principal advantage offered by the present invention is the ability to perform multi-stage *N-point* FFT calculations in a pipelined fashion. *See* Ireland, column 5, lines 48-50.

In light of the foregoing, independent claim 1 is patentable over the references, as neither Suter nor Ireland, alone or in combination, teaches or suggests the above-identified feature of the claims of the present invention. As dependent claim 2 depends from independent claim 1, the dependent claim is patentable over the references for at least the reasons presented for the independent claim, in addition to other reasons.

Regarding claim 2, the Examiner stated that Ireland's figure 8 discloses memory with two banks structure (22, 24). The memories provide a part of the function of an FFT pipeline. The pairs of input data points stored in data memories DM1 and DM2 (22,24) are processed, in order, by a first radix 2 processor stage 30.

In contrast, in the present invention, data is supplied to pipelines with the two-parallel manner. As can be determined from "Permutating method 1 preceding stage," described in the specification of the present invention, each FFT pipeline input is two-parallel manner. So, two pieces of data are supplied (two-bank configuration).

Applicants respectfully submit that in contrast to Suter in which an asynchronous circuit that is free of a global clock is utilized, in the present invention, a synchronous type of circuit including a global clock is employed. Further, the number of the transform means is a divisor of the transform point number M (N = MxM) to obtain the same pipeline width of the preceding and succeeding stages.

Further still, although Ireland discloses an N processing stage of radix 2 processors connected in a pipeline, Ireland does not suggest the M-point radix 2 pipeline FFT, as defined by the present invention.

On page 3 of the Office Action, claim 8 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Suter and Ireland as applied to claim 1 and further in view of what the Examiner described as "applicant admission of prior art." Applicants respectfully submit that the Japanese patent identified in the description cited by the Examiner, that is, Japanese Patent No. 2848134, does not teach or suggest twiddle factor multiplication means including 2a complex multiplication circuits.

In light of the foregoing, claim 8, via independent claim 1, is patentable over the references.

Applicants respectfully submit that independent claim 9 is patentable over the references, as the references fail to teach or suggest, "A Fourier transform apparatus characterized in that the Fourier transform apparatus defined in claim 4 is disposed in parallel in a number equal to a power of "2" . . .."

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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